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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,617	01/02/2002	Amnon A. Strasser	Q67549	6027

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EXAMINER	
IQBAL, NADEEM	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,617	STRASSER, AMNON A.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Mar 26, 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 22 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. "backup memory is selected based on a priority determination, a sensitivity to failure determination, a random algorithm, a round robin algorithm, a weighted round robin algorithm, a least recently used algorithm, a space availability determination or network load balancing determination".

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 52 & 64 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 52 & 64recites the limitation "uninterruptible power supplies" in lines 1 & 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Byrd (U.S. Patent number 4,763,333).

3. As per claim 1, Byrd teaches (col. 2, lines 50-53) a computer system that includes a main system (Fig. 3, numeral 1) that further includes a CPU clearly interpreted as a main control unit, a ROM, interpreted as a main non-volatile memory, and a RAM, interpreted as a main volatile memory. Also includes in Byrd system as shown in fig 3, numeral 3, an AUX ROM, an AUX RAM, AUX control, as clearly equivalent to claimed mirror sub-system components that includes a redundant control unit, a redundant volatile memory, and a redundant non-volatile memory. He also teaches a communication link 21, (Fig. 3) between the main sub-system and the mirror sub-system, thus teaching the communication link as claimed. He also teaches (col. 2, lines 50-52) an uninterruptible power supply having means of supplying electric power when the main power line is interrupted. He thus teaches the limitations pertain to an uninterruptible power supply.

4. As per claims 2 & 3, Byrd teaches (col. 2, lines 66, 67) that the system directs the transfer of the application programs and operating system from the computer's RAM to the auxiliary memory and upon restoration of main AC power, the ROM firmware causes the CPU to reload

the application program and operating system into the computer's RAM. He thus teaches that the main system is capable of functioning as a mirror sub-system, and the mirror sub-system capable of functioning as a main sub-system.

5. As per claim 4, He teaches (Fig. 3, numeral 17) a controller that controls the AUX RAM, he thus teaches a controller embedded in the memory circuit.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrd (U.S. Patent number 4,763,333) in view of Ofek et al., (U.S. Patent number 6,052,797).

8. As per claim 5, Byrd does not explicitly disclose that the controller is a disk controller. Ofek et al., teaches remote data mirroring of data storage systems where two data storage systems are interconnected by a data link for remote mirroring of data, the storage systems include disk controllers (Abstract). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the Ofek system into the system of Byrd to be able to utilize disk storages with disk controllers. This is because the stated inclusion provides a desirable advantage to be able to perform data mirroring which is advantage in data recovery if a data in a primary volume is destroyed, thereby providing motivation for the stated inclusion.

9. As per claims 6 & 7, Byrd teaches a communication link 21, (Fig. 3) between the main sub-system and the mirror sub-system as stated above, and Ofek also teaches a data link for remote mirroring, thus providing a communication link.

10. As per claims 8-10, Ofek teaches (Abstract) that each remotely mirrored volume pair can operate in a selected synchronization mode including synchronous, semi-synchronous, adaptive copy, and remote write pending, thereby providing a single communication link.

11. As per claims 11 & 12, Byrd teaches a communication link 21, (Fig. 3) between the main sub-system and the mirror sub-system as stated above being a processor bus, while Ofek teaches the two data storage systems are interconnected by a data link.

12. As per claims 13 & 14, Byrd teaches (col. 2, lines 57-58) that the power mean may, for example, include a storage battery.

13. As per claim 15, Byrd teaches (col. 2, lines 54-56) that the system includes a monitor circuit which generates signals when the main power supply is interrupted and restored and which monitor the condition of the power supply means, thereby providing means for exchanging status information.

14. As per claim 16, Byrd teaches a communication link 21, (Fig. 3) between the main sub-system and the mirror sub-system as stated above being a processor bus, while Ofek teaches the two data storage systems are interconnected by a data link. Thereby providing the first and second communication links.

15. As per claim 17, Byrd teaches a CPU (Fig. 3), which is well know term used for processor, microprocessor, a controller, a microcontroller, or a computer.

16. As per claim 18, Byrd teaches (Fig. 3) a RAM, which is a volatile memory.

17. As per claim 19, Byrd teaches a ROM (Fig. 3), which is well know in the art to be a non-volatile memory, flash memory, a programmable read only memory and similar of a kind.

18. As per claims 20 & 21, Byrd does not explicitly disclose a control unit periodically storing data from the main volatile memory to a backup memory. Ofek teaches (Abstract) that data written to a primary volume is automatically sent over the link to a corresponding secondary volume, thus performing periodically storing data from the main volatile memory to a backup memory.

19. As per claims 23 & 24, Byrd teaches (col. 2, lines 54-56) that the system includes a monitor circuit which generates signals when the main power supply is interrupted and restored and which monitors the condition of the power supply. He thus teaches to monitor the external voltage level for less than a predetermined level.

20. As per claim 25, Byrd teaches (col. 2, lines 65-68) that when a main power interruption is signaled by the monitor circuit. The program directs the transfer of the application programs and operating system from the computer's RAM to the work saving system's auxiliary memory.

21. As per claim 26, Byrd teaches (col. 3, lines 8-10) that upon reliably restoration of main AC power, the ROM firmware causes the CPU to reload the application program and operating system into the computer's RAM and the state of the CPU to be restored.

22. As per claims 27-29, Byrd teaches (col. 2, lines 54-56) that the system includes a monitor circuit which generates signals when the main power supply is interrupted and restored and which monitors the condition of the power supply. He thus teaches to monitor the external voltage level for a predetermined level.

23. As per claim 30, Byrd teaches (Fig. 3) main volatile memory RAM. This would be well known to be plurality of RAMs.

24. As per claim 31, Byrd teaches (Fig. 3) main non-volatile memory ROM. This would be well known to be plurality of ROMs.

25. As per claim 32, Byrd teaches (col. 3, lines 3-5) that when the output voltage of the power supply means drops low enough, the computer is powered down to conserve the remaining energy of the power supply.

26. As per claim 33, Byrd teaches a device for preventing unintentional loss of data in a computer system, he thus teaches a computer system.

27. As per claim 34, Byrd teaches two data storage systems that are interconnected by a data link for remote mirroring of data, thus forming a network of computers.

28. As per claim 35, Byrd teaches (col. 2, lines 50-53) a computer system that includes a main system (Fig. 3, numeral 1) that further includes a CPU clearly interpreted as a main control unit, a ROM, interpreted as a main non-volatile memory, and a RAM, interpreted as a main volatile memory. Also includes in Byrd system as shown in fig 3, numeral 3, an AUX ROM, an AUX RAM, AUX control, as clearly equivalent to claimed mirror sub-system components that includes a redundant control unit, a redundant volatile memory, and a redundant non-volatile memory. He also teaches a communication link 21, (Fig. 3) between the main sub-system and the mirror sub-system, thus teaching the communication link as claimed. He does not explicitly disclose keeping record of which data was transferred to the backup memory. Ofek et al., teaches (Abstract) the data storage system containing the secondary volume has an indication of the degree of consistency of the secondary volume. It would have been obvious to a person of

ordinary skill in the art to include the mirror data storage system of Ofek into the system of Byrd to be able to keep record of which data was transferred to the backup memory. This is because both inventions are in the same environment of preventing loss of data. The inclusion provides a desirable advantage of providing data mirroring with the inclusion, thus providing motivation for the stated inclusion.

29. As per claim 36, Byrd teaches an AUX ROM, an AUX RAM, AUX control, therefore includes a redundant volatile memory or a main non-volatile memory.

30. As per claim 37, Byrd teaches a ROM (Fig. 3), which is well know in the art to be a non-volatile memory, flash memory, a programmable read only memory and similar of a kind.

31. As per claim 38, Byrd teaches (Fig. 3) main non-volatile memory ROM. This would be well known to be plurality of ROMs.

32. As per claims 39 & 40, Byrd teaches (Fig. 3) main volatile memory RAM. This would be well known to be plurality of RAMs.

33. As per claim 41, Byrd teaches (col. 2, lines 54-56) that the system includes a monitor circuit which generates signals when the main power supply is interrupted and restored and which monitors the condition of the power supply. He thus provides the ability to cease the data transfer upon detection of power failure.

34. As per claim 42, Byrd teaches (col. 2, lines 50-53) a computer system that includes a main system (Fig. 3, numeral 1) that further includes a CPU clearly interpreted as a main control unit, a ROM, interpreted as a main non-volatile memory, and a RAM, interpreted as a main volatile memory. Also includes in Byrd system as shown in fig 3, numeral 3, an AUX ROM, an AUX RAM, AUX control, as clearly equivalent to claimed mirror sub-system components that

includes a redundant control unit, a redundant volatile memory, and a redundant non-volatile memory. He also teaches a communication link 21, (Fig. 3) between the main sub-system and the mirror sub-system, thus teaching the communication link as claimed. He also teaches (col. 2, lines 50-52) an uninterruptible power supply having means of supplying electric power when the main power line is interrupted. He thus teaches the limitations pertain to an uninterruptible power supply. He does not explicitly disclose keeping record of which data was transferred to the backup memory. Ofek et al., teaches (Abstract) the data storage system containing the secondary volume has an indication of the degree of consistency of the secondary volume. It would have been obvious to a person of ordinary skill in the art to include the mirror data storage system of Ofek into the system of Byrd to be able to keep record of which data was transferred to the backup memory. This is because both inventions are in the same environment of preventing loss of data. The inclusion provides a desirable advantage of providing data mirroring with the inclusion, thus providing motivation for the stated inclusion.

35. As per claim 43, Byrd teaches an AUX ROM, an AUX RAM, AUX control, therefore includes a redundant volatile memory or a main non-volatile memory.

36. As per claim 44, Byrd teaches a ROM (Fig. 3), which is well know in the art to be a non-volatile memory, flash memory, a programmable read only memory and similar of a kind.

37. As per claim 45, Byrd teaches (Fig. 3) main non-volatile memory ROM. This would be well known to be plurality of ROMs.

38. As per claims 46 & 47, Byrd teaches (Fig. 3) main volatile memory RAM. This would be well known to be plurality of RAMs.

39. As per claim 48, Byrd teaches (col. 2, lines 54-56) that the system includes a monitor circuit which generates signals when the main power supply is interrupted and restored and which monitors the condition of the power supply. He thus provides the ability to cease the data transfer upon detection of power failure.

40. As per claim 49, Byrd teaches a device for preventing unintentional loss of data in a computer system, he thus teaches a computer system.

41. As per claim 50, Byrd teaches two data storage systems that are interconnected by a data link for remote mirroring of data, thus forming a network of computers.

42. As per claim 51, Byrd teaches (col. 2, lines 50-53) a computer system that includes a main system (Fig. 3, numeral 1) that further includes a CPU clearly interpreted as a main control unit, a ROM, interpreted as a main non-volatile memory, and a RAM, interpreted as a main volatile memory. Also includes in Byrd system as shown in fig 3, numeral 3, an AUX ROM, an AUX RAM, AUX control, as clearly equivalent to claimed mirror sub-system components that includes a redundant control unit, a redundant volatile memory, and a redundant non-volatile memory. He also teaches a communication link 21, (Fig. 3) between the main sub-system and the mirror sub-system, thus teaching the communication link as claimed. He also teaches (col. 2, lines 50-52) an uninterruptible power supply having means of supplying electric power when the main power line is interrupted. He thus teaches the limitations pertain to an uninterruptible power supply. Byrd teaches (col. 2, lines 54-56) that the system include a monitor circuit which generates signals when the main power supply is interrupted and restored and which monitors the condition of the power supply. He thus teaches to monitor the external voltage level for a predetermined level. He does not explicitly disclose turning off the uninterruptible power supply

connected to the main non-volatile memory module or indicate the completion of data transfer. Byrd teaches (col. 3, lines 3-5) that when the output voltage of the power supply means drops low enough, the computer is powered down to conserve the remaining energy of the power supply. It would have been obvious to a person of ordinary skill in the art to realize that he would also turns off the uninterruptible power supply connected to the main non-volatile memory module or indicate the completion of data transfer. This is because Byrd teaches (col. 3, lines 3-5) that when the output voltage of the power supply means drops low enough, the computer is powered down to conserve the remaining energy of the power supply.

43. As per claims 53 & 54, Byrd teaches an AUX ROM, an AUX RAM, AUX control, therefore includes a redundant volatile memory or a main non-volatile memory.

44. As per claim 55, Byrd teaches a ROM (Fig. 3), which is well know in the art to be a non-volatile memory, flash memory, a programmable read only memory and similar of a kind.

45. As per claim 56, Byrd teaches (Fig. 3) main volatile memory RAM. This would be well known to be plurality of RAMs.

46. As per claim 57, Byrd teaches (col. 2, lines 54-56) that the system includes a monitor circuit which generates signals when the main power supply is interrupted and restored and which monitors the condition of the power supply. He thus provides the ability to cease the data transfer upon detection of power failure.

47. As per claim 58, Byrd teaches a device for preventing unintentional loss of data in a computer system, he thus teaches a computer system.

48. As per claim 59, Byrd teaches two data storage systems that are interconnected by a data link for remote mirroring of data, thus forming a network of computers.

49. As per claim 60, Byrd teaches (col. 3, lines 3-5) that when the output voltage of the power supply means drops low enough, the computer is powered down to conserve the remaining energy of the power supply. It would have been obvious to a person of ordinary skill in the art to realize that he would also turns on the uninterruptible power supply if the voltage level is above the predetermined level. This is because Byrd teaches (col. 3, lines 3-5) that when the output voltage of the power supply means drops low enough, the computer is powered down to conserve the remaining energy of the power supply., therefore if the voltage level is above the predetermined level he would clearly turns on the uninterruptible power supply.

50. As per claims 61 & 62, Byrd teaches (col. 2, lines 54-56) that the system includes a monitor circuit which generates signals when the main power supply is interrupted and restored and which monitors the condition of the power supply. He thus teaches to monitor the external voltage level for a predetermined level.

51. As per claim 63, Byrd teaches (col. 2, lines 50-53) a computer system that includes a main system (Fig. 3, numeral 1) that further includes a CPU clearly interpreted as a main control unit, a ROM, interpreted as a main non-volatile memory, and a RAM, interpreted as a main volatile memory. Also includes in Byrd system as shown in fig 3, numeral 3, an AUX ROM, an AUX RAM, AUX control, as clearly equivalent to claimed mirror sub-system components that includes a redundant control unit, a redundant volatile memory, and a redundant non-volatile memory. He also teaches a communication link 21, (Fig. 3) between the main sub-system and the mirror sub-system, thus teaching the communication link as claimed. He also teaches (col. 2, lines 50-52) an uninterruptible power supply having means of supplying electric power when the main power line is interrupted. He thus teaches the limitations pertain to an uninterruptible

power supply. Byrd teaches (col. 2, lines 54-56) that the system include a monitor circuit which generates signals when the main power supply is interrupted and restored and which monitors the condition of the power supply. He thus teaches to monitor the external voltage level for a predetermined level. He does not explicitly disclose turning off the uninterruptible power supply connected to the main non-volatile memory module or indicate the completion of data transfer. Byrd teaches (col. 3, lines 3-5) that when the output voltage of the power supply means drops low enough, the computer is powered down to conserve the remaining energy of the power supply. It would have been obvious to a person of ordinary skill in the art to realize that he would also turns off the uninterruptible power supply connected to the main non-volatile memory module or indicate the completion of data transfer. This is because Byrd teaches (col. 3, lines 3-5) that when the output voltage of the power supply means drops low enough, the computer is powered down to conserve the remaining energy of the power supply.

52. As per claim 65, Byrd teaches an AUX ROM, an AUX RAM, AUX control, therefore includes a redundant volatile memory or a main non-volatile memory.

53. As per claims 66 & 68, Byrd teaches (Fig. 3) main volatile memory RAM. This would be well known to be plurality of RAMs.

54. As per claim 67, Byrd teaches a ROM (Fig. 3), which is well know in the art to be a non-volatile memory, flash memory, a programmable read only memory and similar of a kind.

55. As per claim 69, Byrd teaches (col. 2, lines 54-56) that the system includes a monitor circuit which generates signals when the main power supply is interrupted and restored and which monitors the condition of the power supply. He thus provides the ability to cease the data transfer upon detection of power failure.

56. As per claim 70, Byrd teaches a device for preventing unintentional loss of data in a computer system, he thus teaches a computer system.

57. As per claim 71, Byrd teaches two data storage systems that are interconnected by a data link for remote mirroring of data, thus forming a network of computers.

58. As per claim 72, Byrd teaches (col. 3, lines 3-5) that when the output voltage of the power supply means drops low enough, the computer is powered down to conserve the remaining energy of the power supply. It would have been obvious to a person of ordinary skill in the art to realize that he would also turns on the uninterruptible power supply if the voltage level is above the predetermined level. This is because Byrd teaches (col. 3, lines 3-5) that when the output voltage of the power supply means drops low enough, the computer is powered down to conserve the remaining energy of the power supply., therefore if the voltage level is above the predetermined level he would clearly turns on the uninterruptible power supply.

59. As per claims 73 & 74, Byrd teaches (col. 2, lines 54-56) that the system includes a monitor circuit which generates signals when the main power supply is interrupted and restored and which monitors the condition of the power supply. He thus teaches to monitor the external voltage level for a predetermined level.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (703)-308-5228. After Oct. 15, Examiner telephone number would be changed to (571) 272-3659. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703)-305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI